6. A semiconductor device, comprising:

a substrate having transistor devices;

a plurality of copper interconnect metallization lines and conductive vias defined in each of a plurality of interconnect levels of the semiconductor device, the plurality of copper interconnect metallization lines and conductive vias being isolated from each other by a porous dielectric material; and

a plurality of supporting stubs, each of the plurality of supporting stubs configured to form a supporting column that extends through the plurality of interconnect levels of the semiconductor device.

7. A semiconductor device as recited in claim 6, wherein the plurality of supporting stubs is not electrically interconnected to the plurality of copper interconnect metallization lines and conductive vias.

8. A semiconductor device as recited in claim 6, further comprising:

a passivation layer defined over a topmost layer of the copper interconnect metallization lines and conductive vias.

26. (New) A semiconductor device as recited in claim 6, wherein the plurality of copper interconnect metallization lines and conductive vias define dual damascene structures.

27. (New) A semiconductor device as recited in claim 6, wherein the plurality of supporting stubs further support the passivation layer.

28. (New) A semiconductor device, comprising:

a substrate having transistor devices; and

a plurality of copper interconnect metallization lines and conductive vias defined in each of a plurality of interconnect levels of the semiconductor device, the plurality of copper interconnect metallization lines and conductive vias being isolated from each other by a porous dielectric material.

29. (New) A semiconductor device as recited in claim 28, further comprising:

a plurality of supporting stubs, each of the plurality of supporting stubs configured to form a supporting column that extends through the plurality of interconnect levels of the semiconductor device.

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30. (New) A semiconductor device as recited in claim 29, wherein the plurality of supporting stubs is not electrically interconnected to the plurality of copper interconnect metallization lines and conductive vias.

31. (New) A semiconductor device as recited in claim 28, further comprising:

a passivation layer defined over a topmost layer of the copper interconnect metallization lines and conductive vias.

32. (New) A semiconductor device as recited in claim 28, wherein the plurality of copper interconnect metallization lines and conductive vias define dual damascene structures.

33. (New) A semiconductor device as recited in claim 29, wherein the plurality of supporting stubs further support the passivation layer.